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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,658	HENRY ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities:

3. On page 1, Applicant has incorporated six co-pending US Patent Applications by reference without identifying the applications with a serial number. Please amend the specification to reference the US Patent Applications by serial number.

4. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 9 contains the trademark/trade name x86. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or

trade name. In the present case, the trademark/trade name is used to identify/describe an instruction set architecture employed by Intel microprocessors and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 16, 18-33 and 36-45 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Stiles et al., US Patent 5,163,140.

10. Referring to claim16, Stiles et al. have taught a microprocessor for detecting and correcting an erroneous speculative branch, comprising:

a. an instruction cache, for providing a line of instruction bytes selected by a fetch address, said fetch address provided to said instruction cache on an address bus (Figure 1, ICACHE RAMS, column 5, line 51-column 6, line 12);

b. a speculative branch target address cache (BTAC), coupled to said address bus, for providing a speculative target address of a previously executed branch instruction in response to said fetch address whether or not said previously executed branch instruction is present in said line (column 9, lines 27-58);

c. control logic, coupled to said BTAC, configured to control a multiplexer to select said speculative target address as said fetch address during a first period (column 13, line 47-column 14, line 2); and

d. prediction check logic, coupled to said BTAC, configured to detect that said control logic controlled said multiplexer to select said speculative target address erroneously (column 6, line 59-column 7, line 30, column 16, lines 33-36);

wherein said control logic is further configured to control said multiplexer to select a correct address as said fetch address during a second period in response to said prediction check logic detecting said erroneous selection (column 6, line 59-column 7, line 30, column 16, lines 33-36).

11. Referring to claim 18, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: instruction decode logic, configured to receive and decode said instruction bytes and to specify to said prediction check logic whether a branch instruction is present in said instruction bytes (column 6, line 59-column 7, line 30, column 16, lines 33-36).

12. Referring to claim 19, Stiles et al. have taught the microprocessor of claim 18, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that a branch instruction is not present in said instruction bytes (column 6, line 59-column 7, line 30, column 16, lines 33-36).

13. Referring to claim 20, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of an instruction comprised in said line of instruction bytes; wherein said correct address comprises said instruction pointer of said instruction (column 9, line 35-colum 10, line 10).

14. Referring to claim 21, Stiles et al. have taught the microprocessor of claim 20, as described above, and wherein said instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 35-colum 10, line 10).

15. Referring to claim 22, Stiles et al. have taught the microprocessor of claim 21, as described above, and wherein said location is cached in said BTAC (column 9, line 25-colum 10, line 10).

16. Referring to claim 23, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate a correct branch target address of a branch instruction comprised in said line of instruction bytes based on execution of said branch instruction comprised in said line of instruction bytes; wherein said correct address comprises said correct branch target address (column 6, line 59-column 7, line 30, column 16, lines 33-36).

17. Referring to claim 24, Stiles et al. have taught the microprocessor of claim 23, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said correct branch target address and said speculative target address do not match (column 6, line 59-column 7, line 30, column 16, lines 33-36).

18. Referring to claim 25, Stiles et al. have taught the microprocessor of claim 23, as described above, and wherein said branch instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 25-colum 10, line 10).

19. Referring to claim 26, Stiles et al. have taught the microprocessor of claim 25, ad and wherein said location is cached in said BTAC (column 9, line 25-colum 10, line 10).

20. Referring to claim 27, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: execution logic, configured to receive said line of instruction bytes and to generate a correct direction of a branch instruction comprised in said line of instruction bytes, said correct direction generated based on execution of said branch instruction comprised in said line of instruction bytes (column 6, line 59-column 7, line 30, column 16, lines 33-36).

21. Referring to claim 28, Stiles et al. have taught the microprocessor of claim 27, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said correct direction indicates said branch instruction comprised in said line of instruction bytes is not taken (column 6, line 59-column 7, line 30, column 16, lines 33-36).

22. Referring to claim 29, Stiles et al. have taught the microprocessor of claim 27, as described above, and wherein said branch instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 25-colum 10, line 10).

23. Referring to claim 30, Stiles et al. have taught the microprocessor of claim 29, as described above, and wherein said location is cached in said BTAC (column 9, line 25-colum 10, line 10).

24. Referring to claim 31, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of a next instruction after an instruction comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 35-colum 10, line 10); wherein said correct address comprises said instruction pointer of said next instruction after said instruction (column 9, line 35-colum 10, line 10).

25. Referring to claim 32, Stiles et al. have taught the microprocessor of claim 31, as described above, and wherein said location is cached in said BTAC (column 9, line 25-colum 10, line 10).

26. Referring to claim 33, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising:

a. instruction decode logic, configured to receive and decode said line of instruction bytes and to specify a length of an instruction comprised in said line of instruction bytes, said instruction being at a location of said previously executed branch instruction in said line (Inherent, in order for Stiles et al. to decode the instruction, the decode logic must inherently specify the length of the instruction.).

27. Referring to claim 36, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: instruction decode logic, configured to receive and decode said instruction and to specify which of a plurality of bytes comprising said instruction is an opcode byte (column 7, lines 57-62).

28. Referring to claim 37, Stiles et al. have taught the microprocessor of claim 36, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said control logic controlled said multiplexer to select said speculative target address based on a byte of said instruction other than said opcode byte specified by said instruction decode logic (column 6, line 59-column 7, line 30, column 16, lines 33-36).

29. Referring to claim 38, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of an instruction comprised in said line of instruction bytes, said instruction located at a location of said previously executed branch instruction in said line; wherein said correct address comprises said instruction pointer of said instruction (column 9, line 35-colum 10, line 10).

30. Referring to claim 39, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein an entry of said speculative BTAC caching said speculative target address is invalidated in response to said prediction check logic detecting said erroneous selection (column 6, line 59-column 7, line 30, column 16, lines 33-36).

31. Referring to claim 40, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative BTAC is updated with a direction prediction associated with said previously executed branch instruction, said speculative BTAC being updated in response to said prediction check logic detecting that said control logic controlled said

multiplexer to select said speculative target address erroneously (column 10, lines 10-15, lines 35-48).

32. Referring to claim 41, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative target address is updated in said speculative BTAC in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 10, lines 10-15, lines 35-48).

33. Referring to claim 42, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said prediction check logic comprises an error output, coupled to said control logic, for notifying said control logic of said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 6, line 59-column 7, line 30, column 16, lines 33-36).

34. Referring to claim 43, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein a plurality of pipeline stages of the microprocessor are flushed in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 16, line 33-column 17, line 2).

35. Referring to claim 44, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: an instruction buffer, coupled to said instruction cache, for buffering said line of instruction bytes; wherein said instruction buffer is flushed in response to said prediction check logic detecting that said control logic controlled said multiplexer to

select said speculative target address erroneously (column 16, line 33-column 17, line 2, pipeline, column 13, lines 3-47).

36. Referring to claim 45, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative BTAC and said instruction cache are accessed substantially in parallel (Stiles et al., column 9, line 35-colum 10, line 10, column 2, lines 48-50).

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. Claims 1-6, 10-15, 17, 46-53, and 57-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868.

39. Referring to claim 1, Stiles et al. have taught an apparatus in a microprocessor for detecting that the microprocessor erroneously branched to a speculative target address that is provided by a branch target address cache (BTAC), the apparatus comprising:

a. a storage element, for storing an indication of whether the microprocessor branched to the speculative target address provided by the BTAC (column 5, lines 15-33, column 6, line 59-column 7, line 30) without knowing whether an instruction associated with said indication is a branch instruction (column 9, line 35-colum 10, line 10, All instructions, including non-branch instructions, are checked in the BPC. Since the

addresses are partial address, a hit in the second level BPC does not indicate that the instruction is a branch instruction.);

b. instruction decode logic, configured to receive and decode said instruction (Figure 2, element 160, column 9, lines 35-44); and

c. prediction check logic, coupled to said instruction decode logic, for notifying branch control logic that the microprocessor erroneously branched to the speculative target address if said instruction decode logic indicates said instruction is not a branch instruction and said indication indicates the microprocessor branched to the speculative target address (column 6, line 59-column 7, line 30, column 16, lines 33-36).

d. Stiles et al. have not specifically taught the instruction decode logic, configured to receive and decode said instruction subsequent to the microprocessor branching to the speculative target address. Gochman et al. have taught an instruction decode logic configured to receive and decode said instruction subsequent to the microprocessor branching to the speculative target address (Figures 3 and 4, column 4, lines 13-49) for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the decode unit of Stiles et al., receive and decode said instruction subsequent to the microprocessor branching to the speculative target address, as taught by Gochman et al. (Figures 3 and 4, column 4, lines 13-49), for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time.

40. Referring to claim 2, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above, and wherein said storage element is in an instruction buffer for storing instructions, including said instruction (Stiles et al., column 5, lines 15-33, column 6, line 59-column 7, line 30; Gochman et al., Figure 1, element 53).

41. Referring to claim 3 Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above, and wherein said indication indicates that the microprocessor branched to the speculative target address cached in the BTAC without certainty that said instruction decoded by said instruction decode logic is a same instruction for which the BTAC cached the speculative target address (Stiles et al., column 9, line 35-colum 10, line 10, All instructions are checked in the BPC. Since the addresses are partial address, a hit in the second level BPC does not indicate that the instruction is the same instruction for which the BPC cached the speculative target address.).

42. Referring to claim 4, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above, and wherein said indication indicates that the microprocessor branched to the speculative target address provided by the BTAC in response to a fetch address that selected a line of instructions in an instruction cache (Stiles et al., column 9, line 35-colum 10, line 10).

43. Referring to claim 5, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 4, wherein said indication indicates that the microprocessor branched to the speculative target address in response to said fetch address without certainty whether a previously executed instruction, for which the BTAC cached said target address, is present in said instruction cache line (Stiles et al., column 9, line 35-colum 10, line 10, partial addresses).

44. Referring to claim 6 Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above, and wherein said instruction decode logic is configured to determine a first instruction length of said instruction (Inherent, in order for Stiles et al. to decode the instruction, the decode logic must inherently determine the length of the instruction.).

45. Referring to claim 10, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above, and wherein the apparatus further comprises:

a. address generation logic, coupled to said instruction decode logic, for generating a correct target address of said instruction (column 6, line 59-column 7, line 30, column 16, lines 33-36); and

b. a comparator, coupled to said address generation logic, for comparing the speculative target address provided by the BTAC and said correct target address of said instruction, and for providing a mismatch indicator to said prediction check logic based on said comparing (column 6, line 59-column 7, line 30, column 16, lines 33-36).

46. Referring to claim 11, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 10, as described above, and wherein said prediction check logic is configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said mismatch indicator indicates the speculative target address and said correct target address of said instruction do not match (column 6, line 59-column 7, line 30, column 16, lines 33-36).

47. Referring to claim 12, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above, and wherein the apparatus further comprises: execution logic, operatively coupled to said instruction decode logic, for determining a correct direction of

said instruction, said correct direction specifying whether said instruction is taken or not taken, said execution logic providing said correct direction to said prediction check logic (column 6, line 59-column 7, line 30, column 16, lines 33-36).

48. Referring to claim 13, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 12, as described above, and wherein said prediction check logic is configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said correct direction indicates said instruction is not taken (column 6, line 59-column 7, line 30, column 16, lines 33-36).

49. Referring to claim 14, Stiles et al. have taught an apparatus in a microprocessor for detecting that the microprocessor erroneously speculatively branched to a target address that is provided by a speculative branch target address cache (BTAC), the apparatus comprising:

a. a storage element, for storing an indication of whether the microprocessor speculatively branched to the target address provided by the BTAC (column 5, lines 15-33, column 6, line 59-column 7, line 30) based on an instruction cache fetch address without first determining whether a branch instruction is present in a line of instruction bytes in the instruction cache selected by said fetch address (column 9, line 35-colum 10, line 10, All instructions, including non-branch instructions, are checked in the BPC. Since the addresses are partial address, a hit in the second level BPC does not indicate that the instruction is a branch instruction.);

b. instruction decode logic, configured to receive and decode said instruction bytes in said instruction cache line (Figure 2, element 160, column 9, lines 35-44, column 17, lines 9-27), said instruction decode logic further configured to indicate whether said line

includes a branch instruction (column 6, line 59-column 7, line 30, column 16, lines 33-36, column 17, lines 9-27); and

c. prediction check logic, coupled to said instruction decode logic, for providing an error signal to branch control logic if said indication indicates the microprocessor speculatively branched to the target address and said instruction decode logic indicates said line does not include a branch instruction (column 6, line 59-column 7, line 30, column 16, lines 33-36).

50. Stiles et al. have not specifically taught instruction decode logic, configured to receive and decode said instruction bytes in said instruction cache line subsequent to the microprocessor speculatively branching to the target address. Gochman et al. have taught instruction decode logic, configured to receive and decode said instruction bytes in said instruction cache line subsequent to the microprocessor speculatively branching to the target address address (Figures 3 and 4, column 4, lines 13-49) for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the decode unit of Stiles et al., receive and decode said instruction subsequent to the microprocessor branching to the speculative target address, as taught by Gochman et al. (Figures 3 and 4, column 4, lines 13-49), for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time.

51. Referring to claim 15, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 14, as described above, and wherein the target address is provided by a

speculative call/return stack in the microprocessor rather than the speculative BTAC in response to an indication cached in the BTAC that said line of instruction bytes includes a return instruction (Gochman et al., column 4, lines 13-45) for the desirable purpose of predicting the return address of return from subroutine branch instructions such that the processor does not need to stall while a main memory access occurs (Gochman et al., column 2, lines 24-28).

52. Referring to claim 17, Stiles et al. have taught the microprocessor of claim 16, as described above. Stiles et al. have not specifically taught wherein said second period is subsequent to said first period. However, Gochman et al. have taught wherein said second period is subsequent to said first period (Figures 3 and 4, column 4, lines 13-49) for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Stiles et al., include wherein said second period is subsequent to said first period, as taught by Gochman et al. (Figures 3 and 4, column 4, lines 13-49), for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time.

53. Claims 46-53, and 57-63 do not recite limitations above the claimed invention set forth in claims 1-6, 10-15 and are therefore rejected for the same reasons set forth in the rejection of claims 1-6, 10-15 above.

54. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868 and Fite et al., US Patent 5,142,634.

55. Referring to claim 34, Stiles et al. have taught the microprocessor of claim 33, as described above. They have not specifically taught wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said length of said instruction does not match an instruction length cached in said speculative BTAC for said previously executed branch instruction. However, Fite et al. have taught prediction check logic is configured to determine if said first instruction length does not match a second instruction length that is cached in the BTAC and received therefrom (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24) for the desirable purpose of determining whether the address of the branch instructions has a valid associated entry in the cache. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the branch control logic of Stiles et al. notify said branch control logic that the microprocessor erroneously branched to the speculative target address, using the instruction length comparison concept, as taught by Fite et al., for the desirable purpose of determining branch speculation validity (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24).

56. Referring to claim 35, Stiles et al. have taught the microprocessor of claim 34, as described above, and further comprising: branch target address generation logic, configured to receive said instruction and to generate an instruction pointer of said instruction; wherein said correct address comprises said instruction pointer of said instruction (column 9, line 35-colum 10, line 10).

57. Claims 7, 54, 55, 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868 and Fite et al., US Patent 5,142,634.

58. Referring to claim 7, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 6, as described above. They have not specifically taught wherein said prediction check logic is configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said first instruction length does not match a second instruction length that is cached in the BTAC and received therefrom. However, Fite et al. have taught prediction check logic is configured to determine if said first instruction length does not match a second instruction length that is cached in the BTAC and received therefrom (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24) for the desirable purpose of determining whether the address of the branch instructions has a valid associated entry in the cache. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the branch control logic of Stiles et al. notify said branch control logic that the microprocessor erroneously branched to the speculative target address, using the instruction length comparison concept, as taught by Fite et al., for the desirable purpose of determining branch speculation validity (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24).

59. Claim 54 does not recite limitations above the claimed invention set forth in claims 1-53 and is therefore rejected for the same reasons set forth in the rejection of claims 1-53 above.

60. Referring to claim 55, Stiles et al., in combination with Gochman et al. and Fite et al. have taught the method of claim 54, as described above, and further comprising: invalidating an

entry containing the speculative target address in the BTAC if said length of the presumed branch instruction does not match said instruction length speculatively provided by the branch target address cache (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24).

61. Referring to claim 56, Stiles et al., in combination with Gochman et al. and Fite et al. have taught the method of claim 55, as described above, and wherein said invalidating is performed prior to said branching to said instruction pointer (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24, Stiles et al., column 9, line 35-colum 10, line 10).

62. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868 and Brown et al., US Patent 5,867,701.

63. Referring to claim 8, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 1, as described above. They have not specifically taught wherein said prediction check logic is configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said indication is associated with a byte of said instruction not defined as a valid opcode byte by an instruction set of the microprocessor. However, Brown et al. have taught prediction check logic is configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said indication is associated with a byte of said instruction not defined as a valid opcode byte by an instruction set of the microprocessor for the desirable purpose of flushing out erroneous instructions to avoid a system fault (Brown et al., column 10, lines 45-54). It would have been

obvious to one of ordinary skill in the art at the time the invention was made to have the prediction check logic of Stiles et al. be configured to notify said branch control logic that the microprocessor erroneously branched to the speculative target address if said indication is associated with a byte of said instruction not defined as a valid opcode byte by an instruction set of the microprocessor, as taught by Brown et al., for the desirable purpose of flushing out erroneous instructions to avoid a system fault (Brown et al., column 10, lines 45-54).

64. Referring to claim 9, Stiles et al. in combination with Gochman et al. have taught the apparatus of claim 8, as described above, and wherein said microprocessor instruction set is an x86 architecture instruction set (Stiles et al., Column 4, lines 56-63).

Conclusion

65. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

66. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

67. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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